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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/779,803	02/08/2001	Moinul I. Syed	A0312/7378 (RMA)	5583

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 01/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/779,803	SYED ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) *2,3,7-29,31-35,37,38,40 and 42-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-6, 30, 32-33, 36, 39 and 41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed 11/23/2005. Accordingly, claims 8-29 and 43-45 are withdrawn from consideration, claims 2-3, 7, 31, 37-38, 40 and 42 were canceled, and claims 1, 4-6, 30, 32-33, 36, 39 and 41 are pending for examination. Note claims 8-29 and 43-45 are drawn to an invention nonelected with traverse in Paper filed 10/31/2003. A complete reply to the final rejection must include **cancellation of nonelected claims** or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Information Disclosure Statement

2. The information disclosure statement filed 9/14/2005 has been considered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1, 6, 30, 36, 39 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai (US PAT. 6,131,143) in view of Hanawa et al. (US PAT. 6,282,505 hereinafter Hanawa).

Regarding claim 1, Sakai discloses a multi-way storage type cache memory system comprising an associative cache including a plurality of memory locations (2, 3a-3n, and 5a-5n, figure 1) for storing data and addresses associated with the data, the memory locations being organized as two or more ways (col. 4 lines 29-36) and each address (10, figure 1) presented to the associative cache being compared with the addresses stored in each of the two or more ways (col. 4 line 52 through col. 5 line 15) and wherein at least one controller (9, figure 1) incorporated with a first device (6, figure 1) to access a first way selected from the two or more ways and a second device (7a-7n, figure 1) to access a second way selected from the two or more ways (col. 5 lines 50-63), and the first and second way can be access concurrently by the first and second devices, respectively (col. 6 lines 19-32). Although Sakai does not specifically discloses at least one controller that enables the first device accessing a location in the first way and the second device being block from the accessing the first way during access by the first device, and the second device accessing a location in the second way and the first device being blocked from accessing the second way during access by the second device, Hanawa, in the analogous art, teaches selectors (108 and 118, figure 1) functioning as at least one controller that

enables a first device (100, figure 1) accessing a location in the first way (125, figure 1) and a second device (110, figure 1) being blocked from access the first way during access by the first device, and the second device accessing a location in the second way (135, figure 1) and the first device being blocked from accessing the second way during access by the second device (col. 7 line 23 through col. 8 line 56) in order to execute a plurality of memory access operations without causing a bank access collision. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Sakai in having at least one controller that enables the first device accessing a location in the first way and the second device being block from the accessing the first way during access by the first device, and the second device accessing a location in the second way and the first device being blocked from accessing the second way during access by the second device, as per teaching of Hawana, in order to execute a plurality of memory access operations without causing a bank access collision.

Regarding claim 6, Sakai discloses a multi-way storage type cache memory system comprising an associative cache including a plurality of memory locations (2, 3a-3n, and 5a-5n, figure 1) to sotre data and addresses associated with the data, the memory locations being organized as two or more ways (col. 4 lines 29-36) and each address (10, figure 1) presented to the associative cache being compared with the addresses stored in each of the two or more ways (col. 4 line 52 through col. 5 line 15) and a plurality of cache outputs for providing data retrieved from the memory locations (output lines from 5a-5n, figure 1), a first multiplexer (6, figure 1) and a second multiplexer (7a-7n, figure 1) having multiplexer inputs coupled to at least some of the memory locations and multiplexer outputs coupled to the plurality of cache outputs via a way selector (9, figure 1) so as to enable the first multiplexer (6, figure 1) to select data from a first

way selected from the two or more ways and a second multiplexer (7a-7n, figure 1) to select data from a second way selected from the two or more ways (col. 5 lines 50-63), and the selected data from the first and second ways being provided concurrently on respective ones of the plurality of cache output (col. 6 lines 19-32). Although Sakai does not specifically discloses the second multiplexer being block from the accessing the first way when the first multiplexer selected data from a location in the first way, and the first device being blocked from accessing the second way when the second multiplexer selected data from a location in a second way, Hanawa, in the analogous art, teaches selectors (108 and 118, figure 1) functioning as at least one controller that enables a first device (100, figure 1) accessing a location in the first way (125, figure 1) and a second device (110, figure 1) being blocked from access the first way during access by the first device, and the second device accessing a location in the second way (135, figure 1) and the first device being blocked from accessing the second way during access by the second device (col. 7 line 23 through col. 8 line 56) in order to execute a plurality of memory access operations without causing a bank access collision. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Sakai in having the second multiplexer being block from the accessing the first way when the first multiplexer selected data from a location in the first way, and the first device being blocked from accessing the second way when the second multiplexer selected data from a location in a second way, as per teaching of Hawana, in order to execute a plurality of memory access operations without causing a bank access collision.

Regarding claim 30, the limitations of the claim are rejected as the same reasons as set forth in claim 1.

Regarding claim 36, the limitations of the claim are rejected as the same reasons as set forth in claim 6.

Regarding claim 39, Sakai teaches at least one of the multiplexers (6 and 7a-7n, figure 1) to select one of the first and second addresses as its output while concurrently controlling another multiplexers to select the other of the first and second address as its output (col. 6 lines 20-32), as well as Hanawa (col. 7 lines 23-58).

Regarding claim 41, the limitations of the claim are rejected as the same reasons as set forth in claim 1.

5. Claims 4-5 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai (US PAT. 6,131,143) in view of Hanawa et al. (US PAT. 6,282,505 hereinafter Hanawa) as applied to claims above, and further in view of Liao et al. (US PAT. 6,857,061 hereinafter Liao).

Regarding claims 4-5, the combination of Sakai teaches the first device comprising a processor (410, figure 5) configured and arranged to access the memory locations (for example see Hanawa col. 5 lines 1-16). The combination of Sakai and Hanawa differs from the claimed invention in not specifically teaching the second device including a data transfer engine configured arranged to transfer data between the memory locations and a lower level memory, wherein the data transfer engine comprises a DMA controller. However, Liao, in the analogous art, teaches a microprocessor (10, figure 3) comprising a BIU/DMA (40, figure 3), read as a data transfer engine, configured and arranged to transfer data between the memory locations, i.e., cache line in L2 (36, figure 3) and a lower level memory (12, figure 3) in order to improve

instruction format which may be used in connection with any suitable type of data processor, from microprocessor to supercomputers with a vector processing unit, thereby improving the operational efficiency (see Liao col. 4 lines 33-37). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Sakai and Hanawa including a data transfer engine configured arranged to transfer data between the memory locations and a lower level memory, wherein the data transfer engine comprises a DMA controller, as per teaching of Liao, in order to improve the operational efficiency.

Regarding claims 32-33, the limitations of the claims are rejected as the same reasons as set forth in claims 4-5.

Response to Arguments

6. Applicant's arguments with respect to claims 1, 4-6, 30, 32-33, 36-39 and 41 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chan et al. (US PAT. 6,298,417) discloses a deallocation pipelining circuit for use in a cache memory subsystem (abstract).

Hasslet et al. (US PAT. 5,450,564) discloses a method for cache memory access with separate fetch and store queues (abstract).

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is (571) 272-4183. The examiner can normally be reached on Tue-Fri 7:30 AM-5:00 PM, and alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li
Patent Examiner
Art Unit 2185

BEHZAD JAMES PEIKARI
PRIMARY EXAMINER